Racal 9917

UHF Counter

Reprint

of

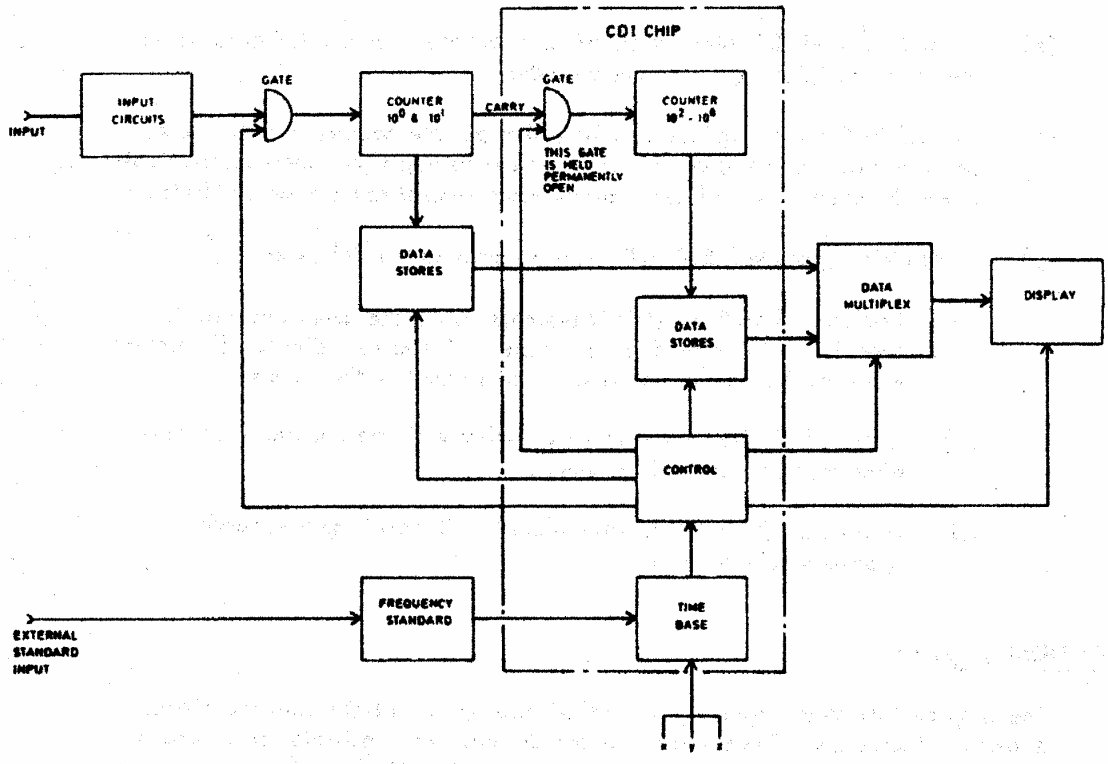
Racal Manual Volume 2
Technical Sections
Layout
and Circuit Diagrams

CHAPTER 3

PRINCIPLES OF OPERATION

BASIC FREQUENCY METER

3.1 A basic digital frequency meter comprises a chain of decade counters feeding b.c.d. data into latched stores. Counting is controlled via a main gate which is opened for a period determined by the time base. Provision is made for resetting the counter and releasing the data for display. In the 9917 the majority of these functions are carried out in the CDI Chip (IC13) which achieves large scale integration (LSI), using the collector-diffusion-isolation process (CDI). Referring to Fig. 3.1, the input signal is gated first into the two off-chip decades which provide the readout data for the 10^0 and 10^1 digits. The 'carry' signal from the 10^1 decade is fed into the counter in the CDI Chip, which provides the readout data for the 10^2 to 10^8 digits. The control system selects the required gating time from the time base, and arranges the correct release of data to the display. The multiplex data output system and display is described in paras. 3.3 to 3.6.



WOH 6217

Basic Frequency Meter

Fig. 3.1

GENERAL CIRCUIT FUNCTIONS

3.2 Outside the CDI Chip, other circuit functions are carried out, as follows:-

(a) Input amplification and signal shaping. Sensitivity control and overload protection. Input (channel) selection.

(b) A nine-digit display system in bit-parallel byte serial (multiplex) form, with data readout available for external use.

(c) Clock (reference) frequency generation using a discrete 5 MHz oscillator circuit, or an optional high-stability temperature controlled oscillator. The reference frequency is doubled to 10 MHz for use in the CDI Chip.

(d) The power supply system operates from a.c. mains and provides supplies of +5V, -5V, +24 and +2V.

(e) For the 10^0 and 10^1 information off-chip counters, associated data stores and data multiplexing stages are provided.

(f) The BURST facility employs circuits which put the counter into the Hold condition with blanked out display. The incoming signal then automatically resets the counter and allows a single measurement to be made and held.

(g) Light emitting diode (LED) indicators are provided as follows:-

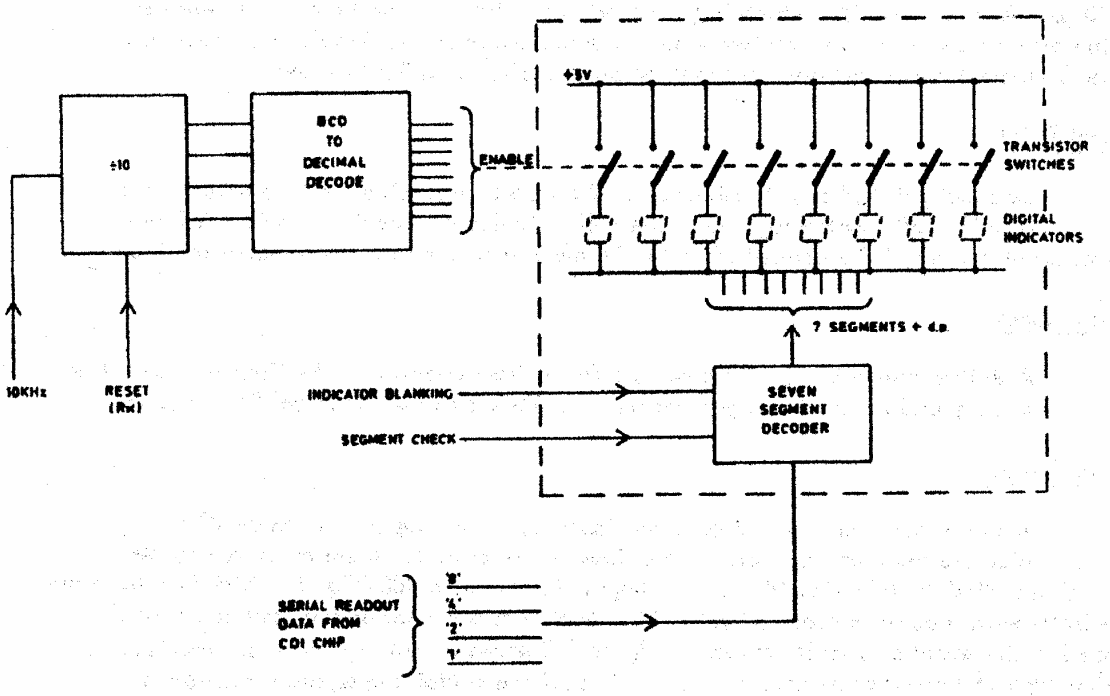
(i) Overflow/Standby: 1LP1 illuminates when the count exceeds the capacity of the nine decade counter. The same indicator illuminates when the POWER switch is set to STANDBY (later models).

(ii) Gate: 1LP3 illuminates in synchronism with the counter main gate when measurement is in progress.

(iii) Overload: 1LP4 illuminates when 'A' Channel input exceeds approximately 5V r.m.s.

Dynamic Display System

3.3 The Display Assembly contains a nine-digit display using light-emitting diodes as numerical indicators. These indicators are driven, via a multiplex stage and a 7 segment decoder, by the b.c.d. data output from the CDI Chip (10^2 to 10^8) together with the multiplexed b.c.d. output from the two off-chip counter (10^0 and 10^1). Each displayed numeral is formed by illuminating an appropriate number of short straight segments. The numeral '8', for example, is formed from 7 segments, where as numeral '5' will only require 5 segments.



Multiplex Display System **Fig. 3.2**

Multiplex Display

3.4 The display data is fed from the data multiplex stage to the Display Assembly via a single four-wire b.c.d. connection. To permit this simple interconnection a parallel-to-serial (multiplex) system is used. The principles are shown in Figure 3.2, although it should be noted that part of the system is in the CDI Chip.

3.5 In the CDI Chip the data stores (digits 10^2 to 10^8) feed in parallel into a b.c.d. four-line output, each store being enabled in sequence for 100 μs. Similarly, the data stores for digits 10^0 and 10^1 also feed in parallel to a multiplex stage where the two four-line outputs are enabled in turn for approximately 100 μs. The enabling signal is a 10 kHz reference derived from the frequency standard.

3.6 The multiplexed data is fed to a 7 segment decoder (IC1) in the Display Assembly, which offers the decoded data to the bank of LED digital indicators. The 10 kHz reference signal is fed to a BCD/Decimal decoder which 'enables' each display LED in turn for 100 μs. A reset pulse (Rx) which is generated in the 10^2 state of the counter, ensures that the display enable is synchronised with the data store readout. Provision is made via IC1 for a segment check and also for blanking out the display in BURST mode.

Decimal Point

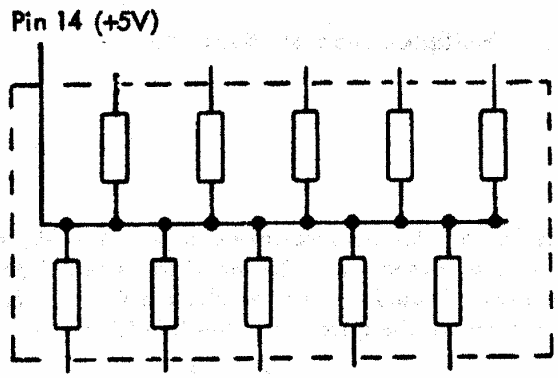
3.7 Decimal point (d.p.) illumination is obtained by encoding the time base control (GATE TIME) switch logic with the digital indicator 'enable' signals. A fixed decimal point position is introduced when the LF Mode is in use to give a readout in Hz.

Control Codes

3.8 A 3-line system is used for time base (gate time) selection. The lines are identified as x, y and z, and the logic coding is in Table 2 in the Technical Specification.

Resistor Arrays

3.9 Many of the integrated circuits are 'open collector' types. For these IC's discrete 'pull-up' resistors are provided in the circuit. These resistors may be mounted in sealed dual-in-line (d.i.l.) packages, for example R88 (Fig. 5) which has thirteen 1k resistors with a common connection to +5V. Such arrays cannot be serviced and must be changed in the event of a faulty resistor. Figure 3.3 shows a 'pull-up' array schematically. Another type of resistor array comprises a d.i.l. package containing separate resistors of identical values, for example R87 which contains eight 220Ω resistors.



D.I.L. Resistor Array Fig. 3.3

CHAPTER 4

TECHNICAL DESCRIPTION

INTRODUCTION

4.1 Apart from some switches and certain items of the power supply, the circuit for the instrument is mounted on one main p.c.b. assembly, with smaller assemblies for the display, reference oscillator and LF Multiplier Assembly. The part numbers and circuit diagrams are as follows:-

Title	Assembly Ref.	Circuit Figure No.
Overall Circuit and Main PCB	19-0808	(Fig. 4
Display Assembly	19-0807	(Fig. 5
LF Multiplier Assembly	19-0797	Fig. 6
5 MHz Standard Oscillator Assembly	19-0834	Fig. 2

LOGIC CIRCUIT SYMBOLS

4.2 Extensive use is made of integrated circuits (IC's) and these are identified by a number and suffix letter. In the circuit description a particular IC pin will be identified by a reference such as 'IC10a/3', which indicates pin 3 on that particular gate. The logic symbols used in the circuits are those found in most manufacturers IC data sheets to which reference should be made if detailed information is required. The CDI Chip IC13 is, however, obtainable only through the Service Department of Racal Instruments Ltd.

'A' CHANNEL INPUT

Introduction

4.3 The circuit is Fig. 4 at the back of the book. The 'A' amplifier operates over the range 40 MHz to 560 MHz with 10 mV sensitivity and automatic gain control (a.g.c.) Overload protection is provided by a relay which interrupts the signal path should the input signal level rise above a pre-determined level. Power supplies of +5V, -5V and +24V are used in the 'A' amplifier circuit.

Signal Path

4.4 The signal path will be described briefly, with more detailed descriptions commencing at para. 4.7. The signal is fed into the main p.c.b. at pin 25, thence via C20 and the contact of the overload relay RLA to a p.i.n. diode attenuator (para. 4.9) and the input of the thick film amplifier IC36. Note that this amplifier has a +24V supply.

4.5 From IC36 the signal is fed via a shunt feedback stage Q6 into parallel paths at C31 and C32. The signal via C31 feeds the a.g.c. detector D10 and D11 and is also used for setting the threshold at which the instrument commences to count (level inhibit).

4.6 The signal at C32 is a.c. coupled to the input of IC26 which is the first counting decade in the 'A' channel. The output from IC26 is fed to the 10^1 counting decade as described in para. 4.26.

'A' Channel Overload Protection

4.7 Although the fast acting a.g.c. system can cope with short term overloads, protection against longer term overload is provided by the protection circuit, which consists basically of the following items, with associated components:-

(a) Relay RLA, which is 'normally open' (i.e. the contact closes only when power is switched on.

(b) The diodes D3/D4 and capacitors C18/C21 which form a detector and voltage doubler.

(c) The operational amplifier IC40.

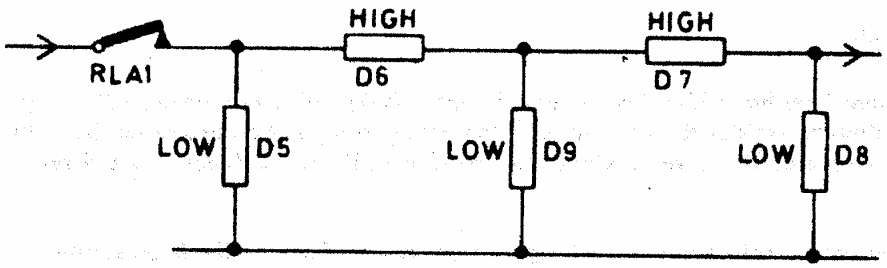
(d) Transistor Q5 which drives the front panel OVERLOAD indicator, LP4.

4.8 The input signal is fed via C18 to the detector D3/D4 and the rectified signal is applied to IC40/2. If the input signal rises above approximately 5V r.m.s., the output at IC40/6 will go high enough to turn off relay RLA, thus interrupting the signal path. At the same time Q5 will turn on, causing the OVERLOAD LED to illuminate.

PIN Diode Attenuator

4.9 The attenuator operates on the principle that the impedance of a diode varies according to the applied bias current. The series elements in the attenuator are diodes D6 and D7, and the shunt elements D5, D8 and D9. Fig. 4.1 below shows the network theoretically, with the diodes represented by resistors. The impedance states refer to a condition of high attenuation.

4.10 If the a.g.c. voltage drives the anode of D9 positive, then current will flow in R32 and the cathodes of D6 and D7 will be reverse-biased, causing a high series impedance. The current in R28 will flow through D5 and that in R39 will flow through D8, causing a low shunt impedance. A low level of a.g.c. voltage will produce the opposite conditions, with variable attenuation over the a.g.c. range.



Theoretical P.I.N. Diode Attenuator Fig. 4.1

Counter Inhibit Circuit ('A' Channel)

4.11 The channel A signal is fed from Q6 via C32 to the 10^{o} counting decade IC26, and also via C31 to a 'level inhibit' stage which automatically inhibits IC26 if the input signal level is too low for reliable counting. The inhibit is produced in IC35a and the threshold is preset by R53. The signal from Q6 is fed via detector D10 to IC35a/1. The reference voltage at IC35a/2 is preset by R53. If the input signal level is unsatisfactory the output at IC35a/12 will be low which will turn off the inverter Q8. The resultant '1' at the collector of Q8 is applied at a 0V level to the reset input of IC19. This forces the $\overline{Q}$ of IC19 to 0V, which inhibits the counter IC26. Instructions for setting-up R53 are given in Chapter 5.

Automatic Gain Control

4.12 At low signal levels the cathode of D10 will be at approximately 0V. As the signal amplitude increases, the voltage at the cathode of D10 (and also at IC35b/7) will become increasingly negative. When the voltage at IC35b/7 is equal to or more negative than IC35b/6, an output will be applied from IC35b/10 to Q7, which feeds current into the p.i.n. diode attenuator at D9. The a.g.c. voltage across R58 is accessible at the two-pin outlet on the rear panel.

'B' CHANNEL INPUT

Signal Input

4.13 Signals in the range 10 Hz to 60 MHz are applied to the front panel 'B' input socket and fed to the SENSITIVITY potentiometer 1R1, which is part of the Display Assembly. From 1R1 the signal is fed via coaxial cable to the 'B' amplifier via pins 32/31 on the main p.c.b. Coupled to the SENSITIVITY potentiometer is the LF SELECT switch; this switch is open in the LF mode and results in a '1' being applied to the signal steering gates (para. 4.18).

'B' Channel Amplifier

4.14 The amplifier has a high impedance FET input (Q1) with overload protection by the clipping resistor R1 together with the gate-drain junction and diode D1. The output from the source of Q1 drives a wideband amplifier IC41, which feeds into emitter follower Q2.

4.15 Transistor Q2 drives a Schmitt trigger shaper stage IC37. IC37b is an emitter-coupled-logic (ECL) line receiver; this is followed by a buffer stage IC37a, which in turn drives a differentiating circuit C17, R22, to produce narrow positive-going pulses at the collector of Q4. From Q4 the signal is fed via the steering gates IC28a and c to the channel B 10° counter IC20.

4.16 The output from Q2 is also applied to the LF Multiplier Assembly via R21 and pin 33 of the main p.c.b., whilst the output signal from the LF Multiplier, is led via pin 37 and the signal steering gates (para. 4.18) to the counter IC20.

CHANNEL SWITCHING

4.17 The required input channel is selected by the front panel INPUT slide switch 1S1, which is part of the Display Assembly. This switch connects the +5V and -5V rails to the appropriate amplifier circuit, and also to the LF Multiplier Assembly. The switch also controls transistor Q11 (Fig. 5) which provides 'channel selected' information; this is applied to the signal steering gates (para. 4.18) and also to the burst mode circuitry (para. 4.37).

SIGNAL STEERING GATES

4.18 A gating network formed by IC14d, IC15a/b/c, IC21 and IC28a/b/c is used to route either the channel B signal direct, the channel B signal via the LF Multiplier Assembly or the 1 MHz (Check) signal to the counter circuitry. The channel A signal is applied direct to the counter (IC26) and A/B selection is controlled within the frequency count and display system; this is explained in para. 4.26.

4.19 The logic control signals applied to the gating network are from the following sources:-

(a) Check/Operate/Reset switch S50 (Check - logic '0')
(Operate - logic '1')

(b) Input select switch 1S1 via Q11 ('channel selected' data)

(c) The LF (switched) position of the SENSITIVITY control (switch is open in LF mode).

4.20 The common output from the gating network is taken from IC28a and is applied to IC20 which is part of the counting chain. The following table indicates the gating paths and assumes that switch S50 is in the OPERATE position except for the CHECK (1 MHz) signal path.

TABLE 3

Signal Gating Paths

Selected Signal	IC28a Input	Signal Path	Logic Source
'B'	IC28a/13	'B' amplifier, IC28c/10	(i) Channel select switch via Q11, IC21d, IC15b, IC21b. (ii) S50 via IC15b, IC21b.
LF Mode	IC28a/1	LF Multiplier, IC15a/13	(i) Sensitivity Control switch (LF) via IC21b. Inhibits IC28c. (ii) S50 via IC15b. (iii) Channel select switch via Q11, via IC21d, IC15b, IC21a.
1 MHz (Check)	IC28a/2	IC15c, IC28b/3	S50 via IC21c, IC28b.

Signal Gating

4.21 The main gate signal is generated and used in the CDI Chip IC13, controlled by the front panel GATE TIME switch (Fig. 5). This signal is inverted by IC30d and is then synchronised before application to the off-chip counters IC26, IC20 and IC16 (Fig. 4). This is accomplished by two D-type bistables IC19, IC27a, which are clocked from the 1 MHz reference. The output from IC27a/5 is applied to signal steering gates IC28c, IC15a and IC28b, whilst the output from IC19/3 gates IC26 via the inhibit at pin 16.

Off-Chip Counter Update and Clear

4.22 The main gate output at the CDI Chip (IC13/19) is also used to generate an update pulse to transfer the data from the off-chip counters to the off-chip data stores. This is achieved by the bistable IC24b. The main gate waveform is applied to the clock input (pin 11), the $\overline{Q}$ (pin 8) goes to '0' and the '1' output from IC25b/6 latches the off-chip data into stores IC8 and IC9. IC24b is then returned to its former state by the inverted phase of the 10 kHz output from IC13/7 via IC30c. The return of IC24b to its former state clocks the Q of IC24a to the '1' state, this generates a clear at the output of IC29b which resets the off-chip counter IC20 and IC16. The bistable IC24a is preset by the 10 kHz clock from the CDI Chip (IC13/7). To prevent the reset (clear) pulse from causing a false count signal at the off-chip counters the carry line at Q10 (Fig. 4) is inhibited because Q9 is turned on (via IC30f) for the duration of the reset pulse.

LF Operation

4.23 On LF operation the gate time is fixed at 1s. This is done by applying a logic code 1-1-0 to the x-y-z pins of the CDI Chip. The 'multiplier select' line (at the upper left hand corner of Fig. 5) is at '1' in LF mode. This is applied direct to IC29c and via inverter IC33f to IC18a and IC18b, giving 1-1-0 at pins 8, 9 and 10 of IC13. The decimal point in the display is automatically selected to provide a readout in 'Hz'. This is done by disabling the normal d.p. selection at IC34a, b and c, which allows the state of IC32d to determine the decimal point position, as described in para. 4.32.

4.24 Display Segment Check. This is obtained by selecting CHECK and INPUT 'A'. Switch S50 (Check position) applies a '0' to IC21c; this is inverted and applied to IC14d/12. The INPUT switch (in position 'A') turns off Q11 which puts a '1' on IC14d/13. The resultant '0' from IC14d/11 is fed to IC1/3 on the display p.c.b. to illuminate all segments.

FREQUENCY COUNT AND DISPLAY SYSTEM

4.25 The display data for digits 10^0 and 10^1 is generated by the off-chip counter IC26 and IC16 (Channel A) or IC20 and IC16 (Channel B), with associated data stores IC9 and IC8 respectively. This data is applied to the data selector (multiplex) stage IC7, and then, together with the 10^2 to 10^8 display data from the CDI Chip (IC13 pins 15 to 18) to a further multiplex stage, IC6. The 4-line b.c.d. output from IC6 is then fed to the 7 segment decoder, IC1. (Fig. 5).

Counter Selection

4.26 The selection of decade counter IC26 (Channel A) or IC20 (Channel B) is controlled by the front panel INPUT switch 1S1 which applies +5V and -5V supplies to the input channel selected. For Channel A, 1S1 removes the +5V from Q11 which turns off and applies a '1' to IC21d. The '0' at IC21d/13 is inverted by IC14a to open gate IC14b and the carry output at IC26/11 is applied to the input of IC16. At the same time, the '0' at

IC21d/13 is applied as a load input to IC20, at pin 1; this inhibits the counting action of IC20 and causes the data at the A, B, C and D inputs (from IC26) to be transferred directly to the QA, QB, QC and QD outputs respectively, and so to the data store IC9.

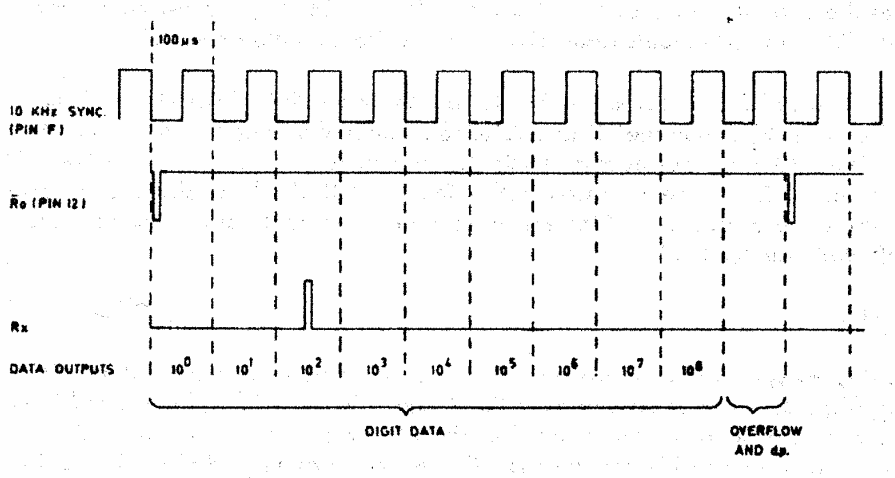
4.27 When Channel B is selected, Q11 is turned on by the INPUT switch, a '0' is applied to IC21d, and the '1' at IC21d/13 is applied as a count enable input to IC20 at pin 1. The B Channel pulses from IC28a/12 are counted by IC20, and the QA, QB, QC, QD output data is fed to the data store IC9. The '1' at IC21d/13 is also used to open gate IC14a for the carry output from IC20 (taken from the QD output, pin 12) which is fed to the other off-chip counter IC16.

Data Synchronising

4.28 The display system is synchronised by the Rx output signal at pin 14 of the CDI Chip (Fig. 5). This is used to reset the decade divider IC38, which is fed from the 10 kHz reference frequency output at pin 7 of the CDI Chip. This results in a '0' output at pin 1 of the 4-line to 10-line decoder IC39 which turns on Q18 via R87 pins 16 and 1. The 10^2 digital indicator is thus enabled and the digit determined by the 7 segment decoder IC1 is displayed. This synchronising pulse is called Rx in Fig. 4.2. The digital indicators for digits 10^3 to 10^8 are then enabled in sequence for 100 µs periods by the '1' to '6' outputs of IC39 (pins 2 to 7). The '8' output from IC39/10 then enables the 10^0 digital indicator via Q16, and at the same time changes the selection state of both IC6 (via IC3d) and IC7 (via the data select line) to allow the data from the off-chip store IC9 to be applied to the 7 segment decoder IC1. Similarly, the '9' output from IC39/11 then enables the 10^1 digital indicator via Q17 and R89, the selection state of IC6 is maintained by IC3d, and the data select line reverts to its former state to allow data from the off-chip store IC8 to be applied to the seven segment decoder IC1.

Rear Data Output

4.29 The data output from IC6, pins 10 to 13, is fed to IC5 which transmits the data via the inverters IC1a, f, e and d, producing $\overline{1}$ - $\overline{2}$ - $\overline{4}$ - $\overline{8}$ data at the rear edge connector. The decimal point information to the edge connector is selected by IC5 during the '7' output state and is given in kHz for all ranges, encoded by IC18d/c, IC34d and IC29a. The $\overline{Ro}$ synchronising output is generated by differentiating the leading edge of the '8' state output in C64 and R86/R100. Thus the timing of the data output is as shown in Fig. 4.2.



Data Sequence Diagram Fig. 4.2

DECIMAL POINT SELECTION

4.30 The decimal point (d.p.) in the required display LED is illuminated by turning on the common d.p. cathode driver transistor Q27 at the same time as the anode of the required digit is turned on. The system operates by encoding the gate time selection (switch S1) with the display 'digit enable' signal. Transistor Q27 is controlled via the gates of IC32 (a, b, c and d), IC34 (a, b and c) and inverters IC33a, b, c and f. It is also controlled by the multiplex reference signals from IC39; these lines are at '1' except when the digit they control is illuminated. The d.p. system is explained by an example, as follows.

4.31 Assume, for example, that the GATE TIME switch selection requires the 10^4 d.p. to be displayed (10 second gate time selected). Wafer S1R applies a '1' to IC34a/1, and a '1' is already on IC34a/2 via inverter IC33f (LF Multiplier not selected). The resultant '0' at IC34a/3, inverted by IC33a, produces a '0' at IC32a/3, and Q27 is held off. When the 10^4 digit line is enabled, the '0' at IC32a/1 results in a '1' at IC32a/3 open collector. This can occur because one input at each of the other 'wired-OR' gates is a '0'. Thus Q27 turns on. The links LK1 and LK2 in the collector circuit of Q27 are fitted in later versions of the Display Assembly to permit the use of different types of LED indicator. See NOTE on circuit diagram Fig. 5. The earlier and later versions of the Display Assembly are not interchangeable.

4.32 When the LF Multiplier is in use the decimal point is fixed. The '1' on the multiplier select line turns off gates IC34a, b and c via inverter IC33f and allows IC32d to turn on Q27 whenever the 10^2 digit is 'enabled'.

OVERFLOW/STANDBY INDICATOR

4.33 The 10 kHz enable signal for the 10^8 digit (IC39/10) is also applied to the set/reset bistable IC12 where it is stored. When the 10^8 decade overflows, a signal from pin 16 of the CDI Chip triggers the set/reset bistable and the OVERFLOW indicator (1LP1) is turned on. This LED is also used as the STANDBY indicator as described in para. 4.62.

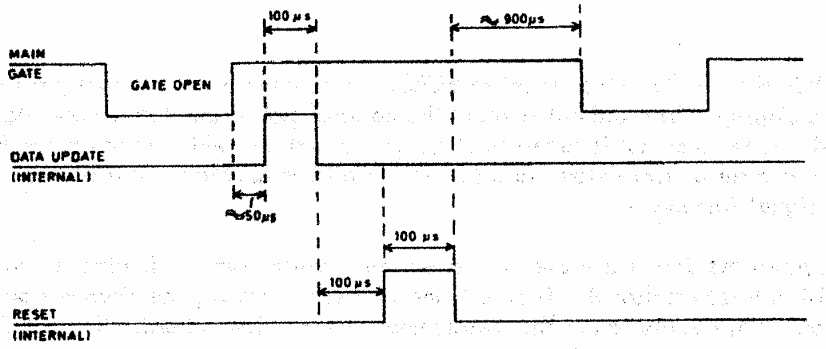
GATE INDICATOR

4.34 The LED GATE indicator(1LP3) illuminates in synchronism with the counter main gate when measurement is in progress. The main gate waveform at IC13/19, which goes negative when the gate is open, illuminates the LED via IC30d and IC10c during the 'gate open' periods.

HOLD/RESET

Automatic Reset

4.35 Automatic reset for digits 10^2 to 10^8 is generated and applied within the CDI Chip, whilst the off-chip counters (digits 10^0 and 10^1) are automatically reset by IC24 (para. 4.22). A timing diagram for the control sequence (as used within the CDI Chip) is given in Fig. 4.3.



Control Sequence Diagram Fig. 4·3

Manual Reset

4.36 Manual hold/reset logic signals are applied to the CDI Chip (IC13/13). The logic requirements for IC13 are:-

(i) Hold is obtained by logic '1'.

(ii) A free-running (unlatched) counter by logic '0'.

(iii) Counter stages are reset on a transition from '1' to '0'.

4.37 To obtain manual reset the switch S50 is pressed to RESET and released. Reset occurs at the moment of release. When the switch is pressed an earth (logic '0') is applied to IC31a/1, which triggers the monostable and also applies a '1' level to IC13/13 via IC25a, IC30a and IC23b. The monostable period also applies a '0' to IC25a/2, covering the period of possible switch contact bounce at IC25a/1. The CDI Chip is now in the 'hold' condition.

4.38 Release of the RESET switch produces a transition from '1' to '0' at IC13/13, thus generating reset. The same transition operates monostable IC31b/10 which applies a '0' pulse via IC29d to IC13/4, thus unlatching the data stores at the same time as the counter stages are reset to '0', thus providing an 'all zero' display.

4.39 The off-chip counters are reset when the monostable IC31b triggers as described in the previous paragraph. The Q output ('1') is inverted in IC29b to reset (clear) IC20 and IC16 (Fig. 4). The unlatch signal at IC29d/13 is applied via IC25b to update (unlatch) the off-chip data stores IC8 and IC9.

BURST MODE

Summary

4.40 When the MODE switch is set to BURST the counter is automatically set to HOLD, the display is blanked out (except the decimal point) and the counter data stores are unlatched. When a signal is received it triggers a bistable which removes the Hold from the counter after a brief delay, to allow the amplifier to settle. The counter then measures the signal frequency.

4.41 Because the data stores are unlatched the counting process is visible, commencing with a brief display of 'all zeros' immediately following the change from hold to reset condition. On completion of the measurement the display is held. If the RESET is pressed and released this again clears the counter for a further burst measurement.

Burst Circuit Description

4.42 When the MODE switch is set to BURST (provided LF is not selected) the earth is removed from the collector of Q15, thus applying a '1' to IC29d/11, IC23a/2, IC10d/12 and IC24a/2.

NOTE: Transistor Q15 is normally off. If LF and Burst modes are selected simultaneously, the '1' on the multiplier select line will turn on Q15, thus inhibiting Burst.

4.43 The '1' at IC23a/2 will open that gate and also put a 'hold' on IC13/13. The other inputs to IC23a are also at 1; IC23a/1 receives a '1' via IC33d from the detector Q25 (para. 4.47) and IC23a/13 is held at about 2.5V by the junction of R73 and R74. At the same time, the '0' output from IC29d/13 unlatches the off-chip data stores via IC25b, and also unlatches the CDI Chip data stores via IC13/4. The '1' at IC24a/2 inhibits the automatic reset of the off-chip counters (para. 4.22).

4.44 After selecting BURST mode, the operator selects manual reset; this clears the bistable IC27b, but does not disturb the hold condition of the counter. The manual reset produces a '1' at IC27b/8 which is applied to IC10d/13. The '0' from IC10d/11 blanks the display digits via the seven segment decoder IC1/4.

4.45 The Channel A burst signal is applied to the preset input of IC27b via IC23c, whilst for Channel B, the input is applied to the clock of IC27b. When either Channel burst signal is received the bistable IC27b changes state and the $\overline{Q}$ output goes to '0' which via IC33e removes the clear from IC22. This $\overline{Q}$ signal is also fed from IC33e/10 to IC25c/9. When Channel B is selected IC25c is enabled, which produces a delay by causing IC22/12 to go briefly to '0', then recover to '1'. This prevents IC22 from being immediately clocked by the 10kHz signal at IC22/11, thus allowing settling time for the 'B' amplifier.

4.46 When IC22/12 returns to '1' the 10kHz clock toggles IC22, causing the $\overline{Q}$ to go to '0', putting a '0' on IC23a/13, thus applying a '0' to IC13/13 which resets the counter in the CDI Chip and allows measurement to commence. Capacitor C50 with R73 differentiates the $\overline{Q}$ output from IC22/8, thus producing the narrow reset pulse, after which the counter returns to the Hold condition, thus the display is held after a single gate time.

Function of Q25 and Q26

4.47 Transistor Q25 and associated diodes D33/D21, provide an interlock facility which ensures that the counter and multiplex system is correctly set for 'burst' reception. Q25 monitors the output of IC38 and, via IC33d, IC23a and IC23b, holds the counter in a free-running condition until IC38 is operating in the correct sequence.

4.48 A secondary function of Q25 is to blank out the display if the 10kHz multiplex reference signal fails. Such failure would cause a display LED to be continuously illuminated. Any loss of drive from IC38 to Q25 will apply a '0' to the seven segment decoder (IC1/4) thus blanking the display. At the end of each main gate period the negative edge is passed into R93, R94, C61 and Q26, which produces a pulse that then blanks the display for approximately 1ms whilst the multiplexed display is re-synchronising with a circuit in the CDI Chip.

FREQUENCY STANDARD

Frequency Standard Options

4.49 These are listed in the Technical Specification as 04A, 04B and 04C. The instrument is normally supplied with 04A. The circuit and component layout diagram for Option 04C is Fig. 2.

4.50 No circuit or parts information is provided for the ovened oscillators. In the event of a fault these units should be returned to Racal Instruments, or authorized agent, for exchange or repair.

Frequency Doubler

4.51 The 5MHz reference from the internal frequency standard is fed to the shaper Q28 on the main p.c.b., and the square wave output is fed via an inverter IC11e, to the digital doubler formed by IC11c and d, and IC17. The 10MHz from IC17a/3 is fed to IC13/5. All further processing of the reference signal is carried out within the CDI Chip.

1MHz Reference Output

4.52 The 1MHz reference is fed from the CDI Chip (IC13/6) via the buffer IC14c to the 1MHz BNC output socket on the rear panel.

External Standard Input

4.53 A 1MHz external reference can be fed in via the rear panel BNC socket to the buffer amplifier Q12 on the main p.c.b., thence to the CDI Chip (IC13/20). When this signal is connected the instrument automatically changes to external standard operation.

LF MULTIPLIER ASSEMBLY

Summary

4.54 Frequency multiplication is achieved by a voltage controlled oscillator which runs at 100 times the input frequency. The divided oscillator frequency is phase-compared with the input frequency to provide fine control of the oscillator signal.

Circuit Description

4.55 The LF signal is applied to the 'B' input and fed through the 'B' amplifier (Fig. 4) into the LF Multiplier p.c.b. (Fig. 6). Referring to Fig. 6 the signal is fed via C1 into the Operational Amplifier IC1, which functions as a Schmitt Trigger. With an input of approximately 400mV peak-to-peak applied to IC1 an output of approximately 6V peak-to-peak will be fed into IC2/14.

4.56 IC2 contains a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL). The factors controlling the oscillator frequency are:-

(1) The voltage on pin 9 of IC2.

(2) The resistance between pin 11 and the negative rail.

(3) The capacitance between pins 6 and 7.

(4) The output of the phase comparator at pin 13.

4.57 The oscillator output at IC2/4 is fed via Q3 to a dual decade divider IC3. From IC3/13 the divided signal is fed back via Q2 to pin 3 of IC2, where it is compared in phase with the original signal at pin 14. This phase comparison voltage is fed via pin 13 and R4 to pin 9, to pull the oscillator to a frequency which is a precise multiple of the input frequency.

NOTE: When fitting a new LF Multiplier p.c.b. check that it is fitted with link LK2. (See circuit diagram Fig. 6).

POWER SUPPLY

4.58 The a.c. supply is fed in via a 3-pin fixed plug on the rear panel, thence via the anti-surge fuse FS50 to the transformer T50. The transformer tappings are arranged to suit the local supply voltage as shown in Fig. 5.1 in Chapter 5. The output at secondary winding 'A' is rectified by the potted bridge rectifier D50, which is mounted on the rear panel for adequate heat dissipation and supplies the +5V regulator Q50. The supply to the -5V regulator Q51 is provided by the discrete diode bridge D29-D32. The reservoir capacitors are C100 and C101.

+24V Supply

4.59 The output at secondary winding 'C' is rectified to provide the +24V supply; diodes D25-D28 form a bridge rectifier, and transistors Q31/Q32 form a conventional voltage comparator to regulate the current in Q30. Smoothing is provided by C74 whilst C73 decouples the comparator reference input which is taken from the switched +5V supply (para. 4.60).

+5V Stabilization

4.60 The reference is provided from the +5V rail by zener diode D23 which is connected to the comparator IC4a/2. The other input to the comparator (IC4a/1) is from the 0V rail. The comparator function is to ensure that the 0V rail is maintained 5.1V below the voltage of the +5V rail. Any change from this state will cause IC4a to apply a signal to Q29 which will regulate the current in Q50 to restore the correct condition. Capacitors C52 and C71 stabilize the system.

-5V Stabilization

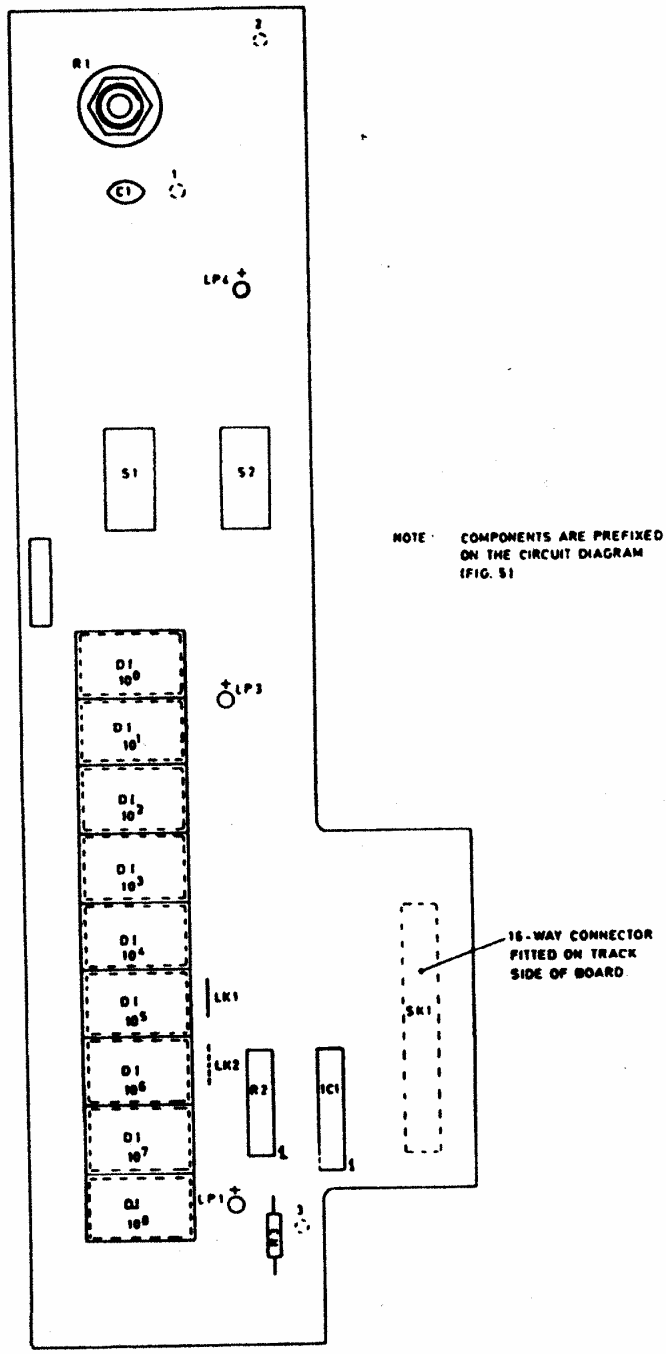
4.61 The -5V stabilizing comparator is IC4b, in which both inputs should be at 0V when conditions are correct. IC4b/7 is connected to the 0V rail and IC4b/6 to the mid-point of a potential divider (R112, R113 and R114) which is connected between the stabilized +5V rail and the -5V rail. If the level at IC4b/6 departs from 0V then a correcting signal from IC4b/10 will regulate the current in Q51 to correct the error. Capacitor C69 ensures that any ripple on the +5V supply will not affect the -5V supply stability via IC4b.

OFF/STANDBY/ON Switching

4.62 The +5V, -5V and +24V supplies to the instrument are switched by the POWER switch S51. In the OFF position, S51b open circuits the anode of the +5V supply reference diode D23. S51a applies an earth to the +24V comparator transistor Q31 via R115 and also to the reference input of the -5V regulator via R112, R113. In the STANDBY oosition, S51b completes the circuit for D23 which activates the regulated +5V supply. The -5V (H) supply is connected to the OVERFLOW indicator (1LP1) which also serves as a STANDBY indicator due to the earth return path provided by S51a via R3, when on STANDBY. When S51 is set to ON, however, this path is broken, 1LP1 is extinguished, and the stabilized supplies are fed to the instrument.

CDI Chip 2V Supply

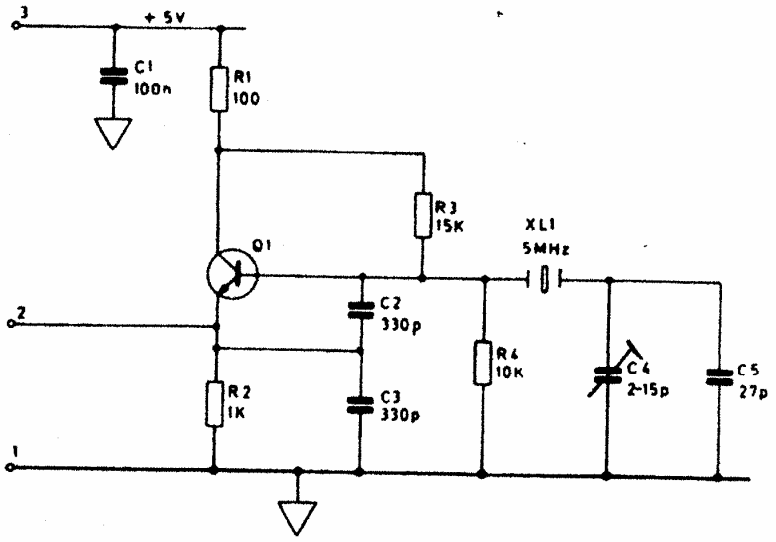
4.63 A stabilized +2V supply is derived from the +5V rail via the regulator Q13 which is controlled by Q14 from a reference voltage provided by the CDI Chip at IC13/11.

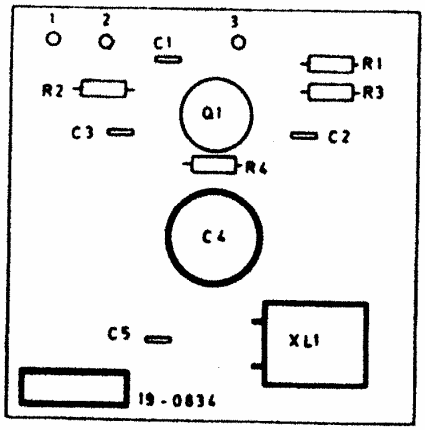


V.OH 6217 | 19-0807
1 | 2 | 3

Component Layout
Display Assembly 19-0807

Fig. 1





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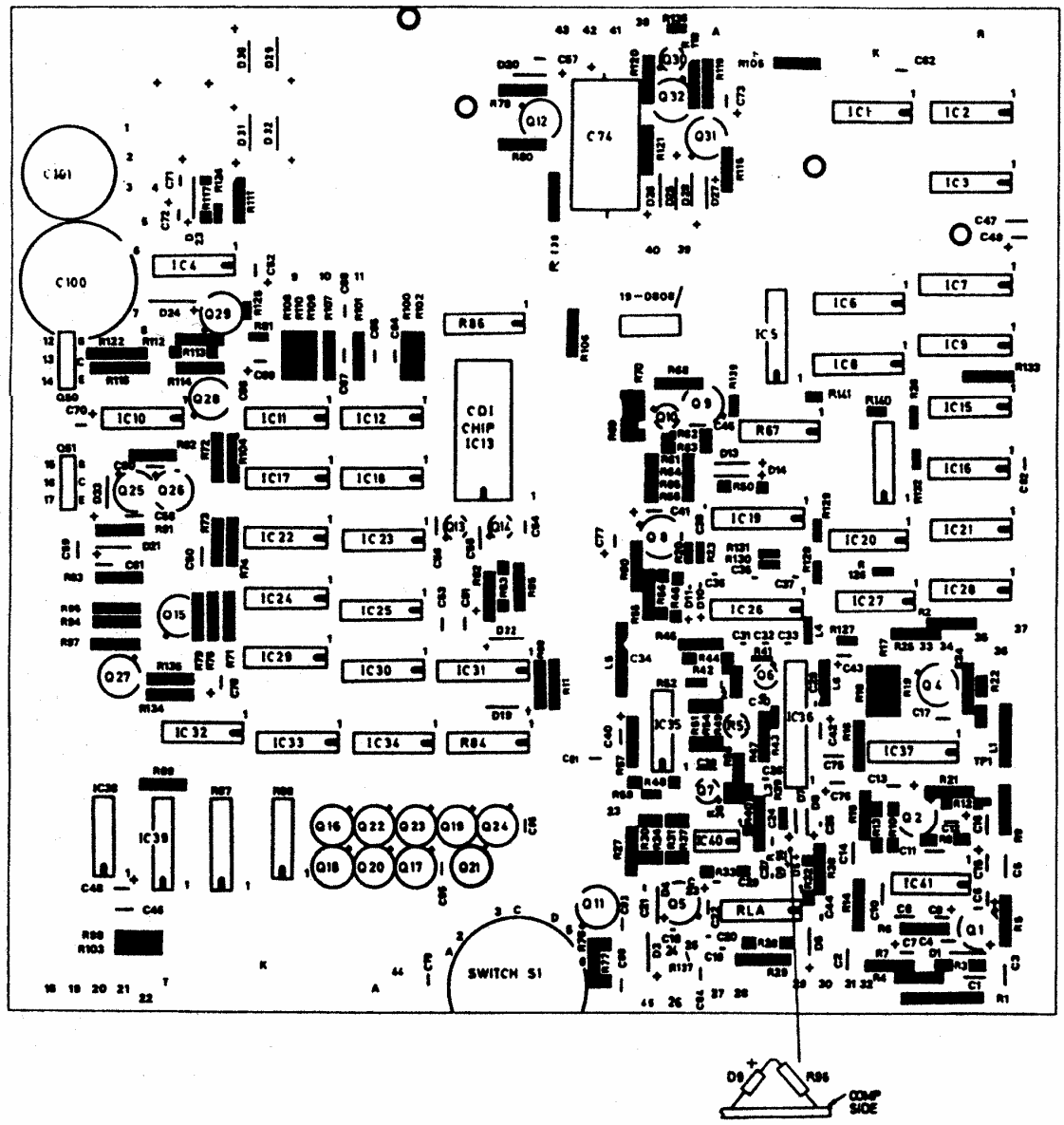
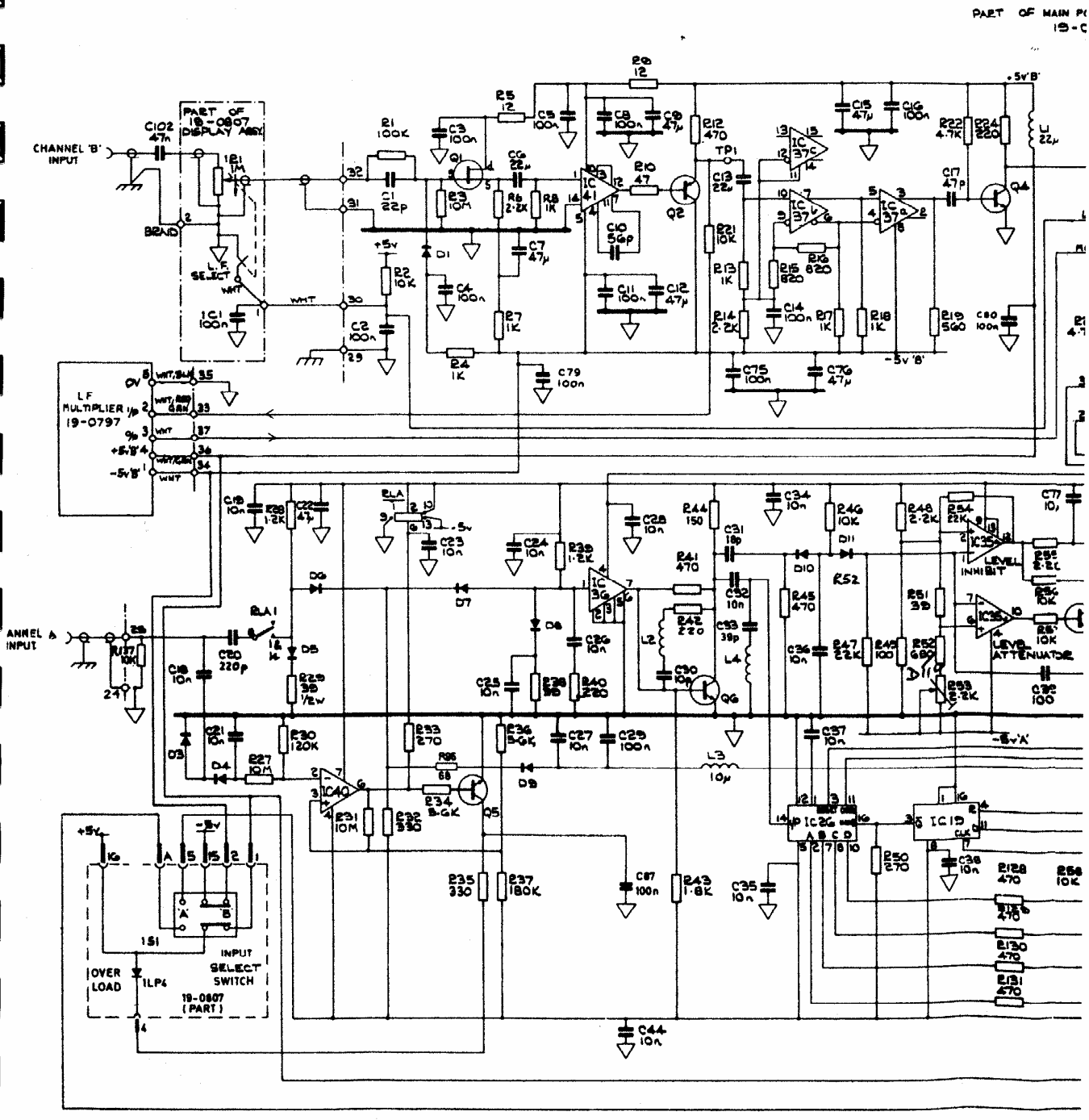
Circuit And Layout
5MHz Oscillator PCB 19-0834

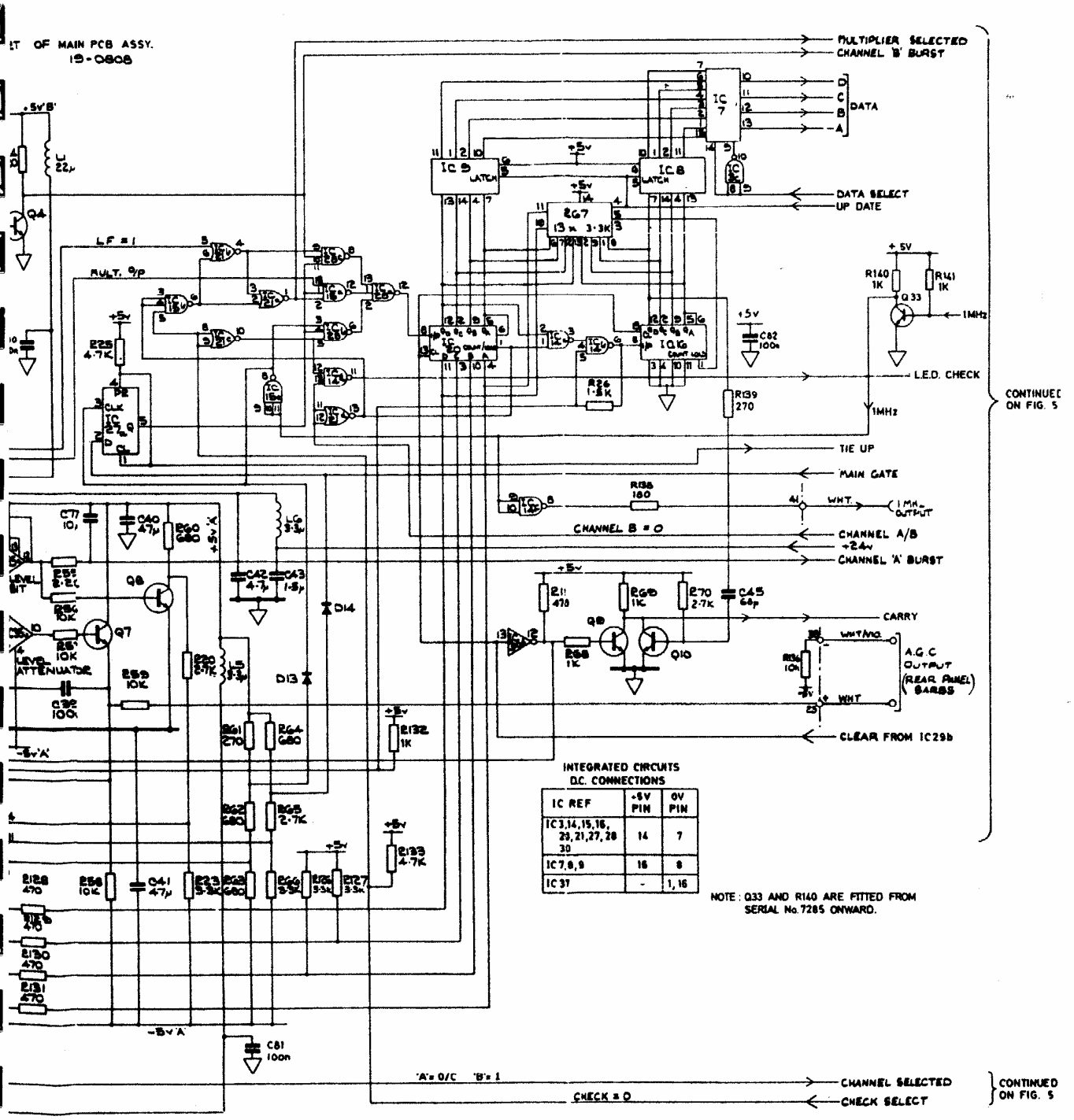
Fig. 2



Component Layout:
Main PCB 19-0808

Fig. 3

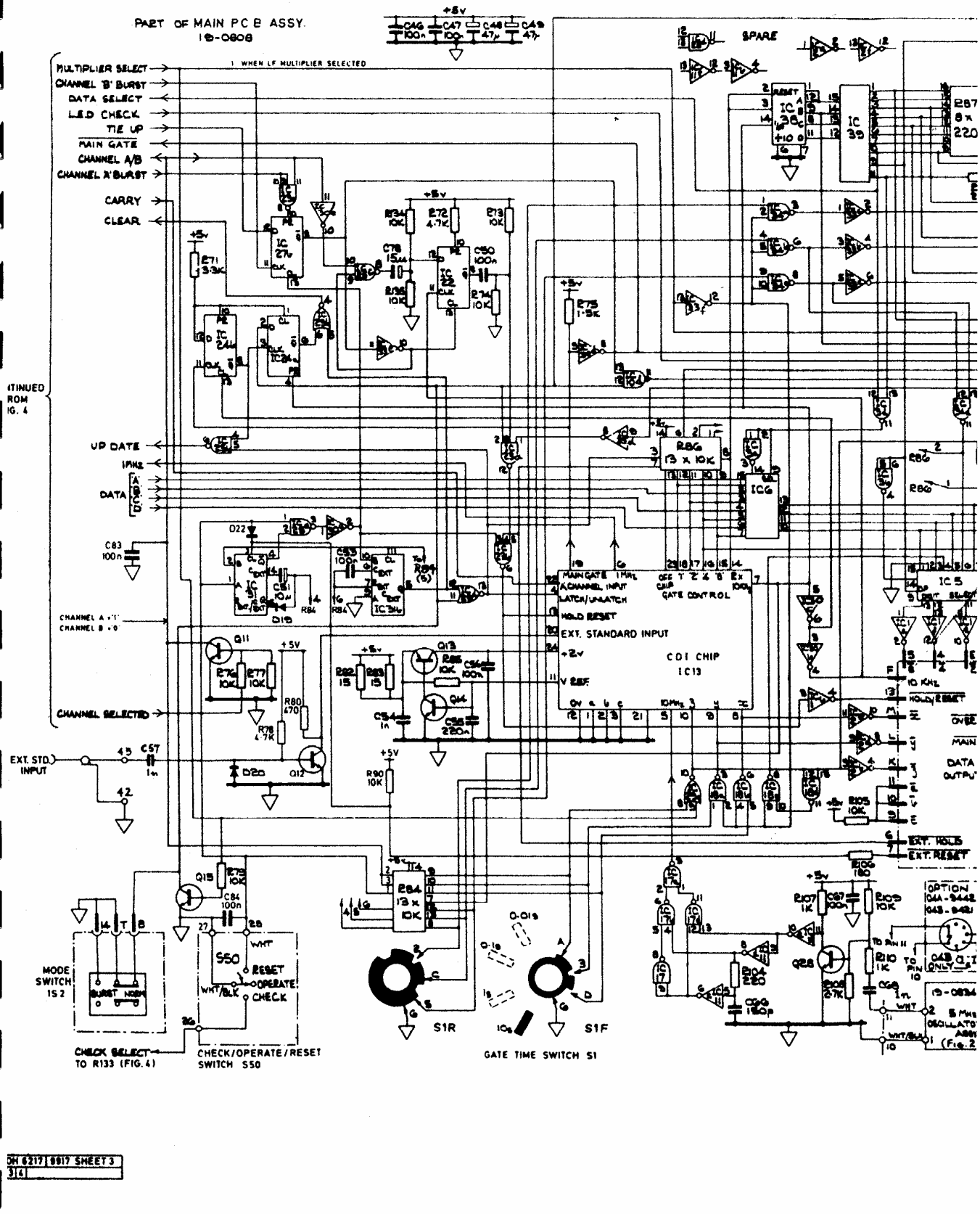

PART OF MAIN PC
19-0
CHANNEL 'B' INPUT
PART OF 19-0807 DISPLAY ASSY.
BRAND
L.F. SELECT
LF MULTIPLIER I/p 19-0797
0V
0v
+5v'B'
-5v'B'
+5v
-5v
TP1
LEVEL INHIBIT
LEVEL ATTENUATOR
CHANNEL A INPUT
INPUT SELECT SWITCH
OVER LOAD
19-0807 (PART)
-5v'A'
DM 6217 | 8817 SHEET 2
3 4 5 6

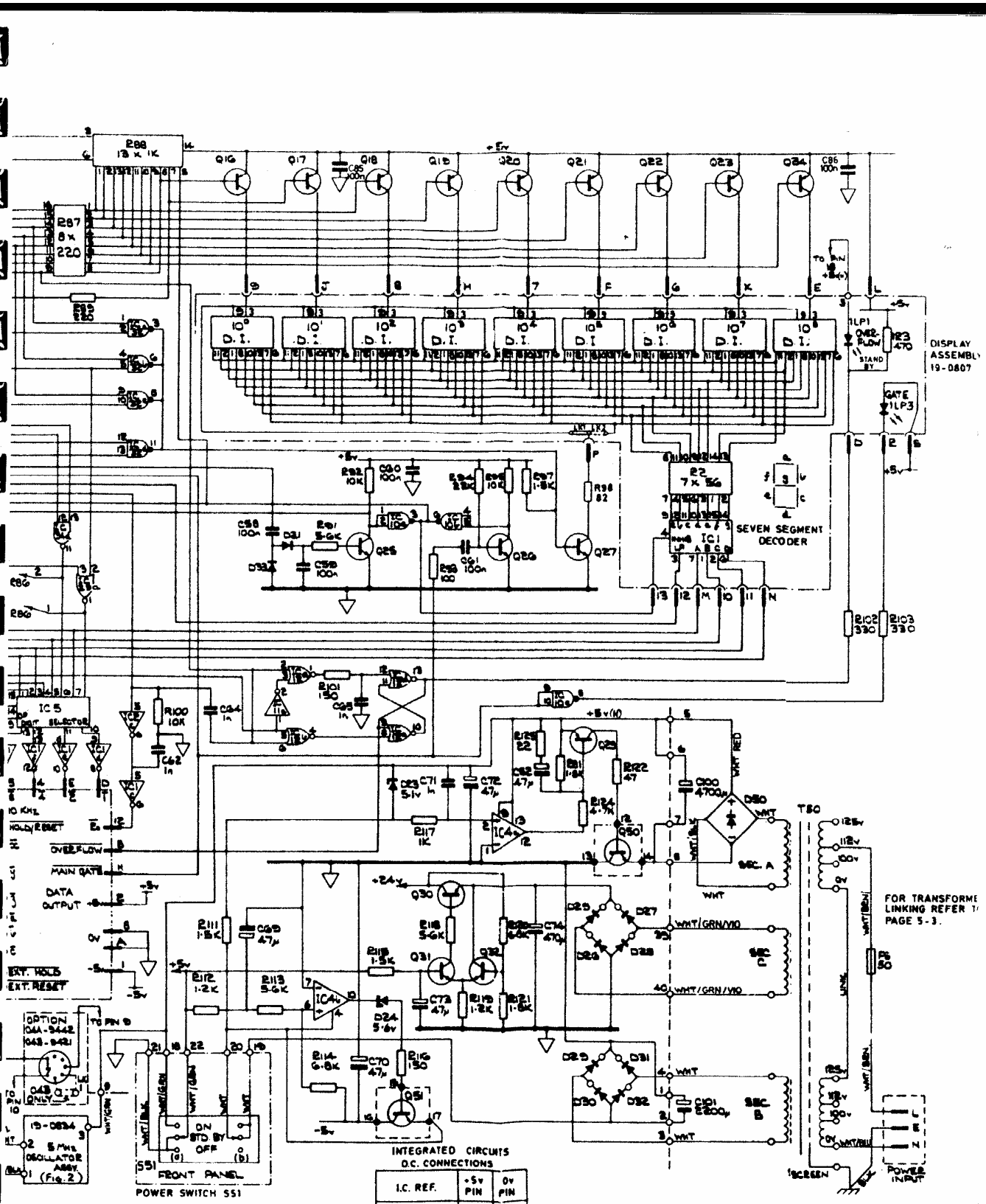


INTEGRATED CIRCUITS
D.C. CONNECTIONS

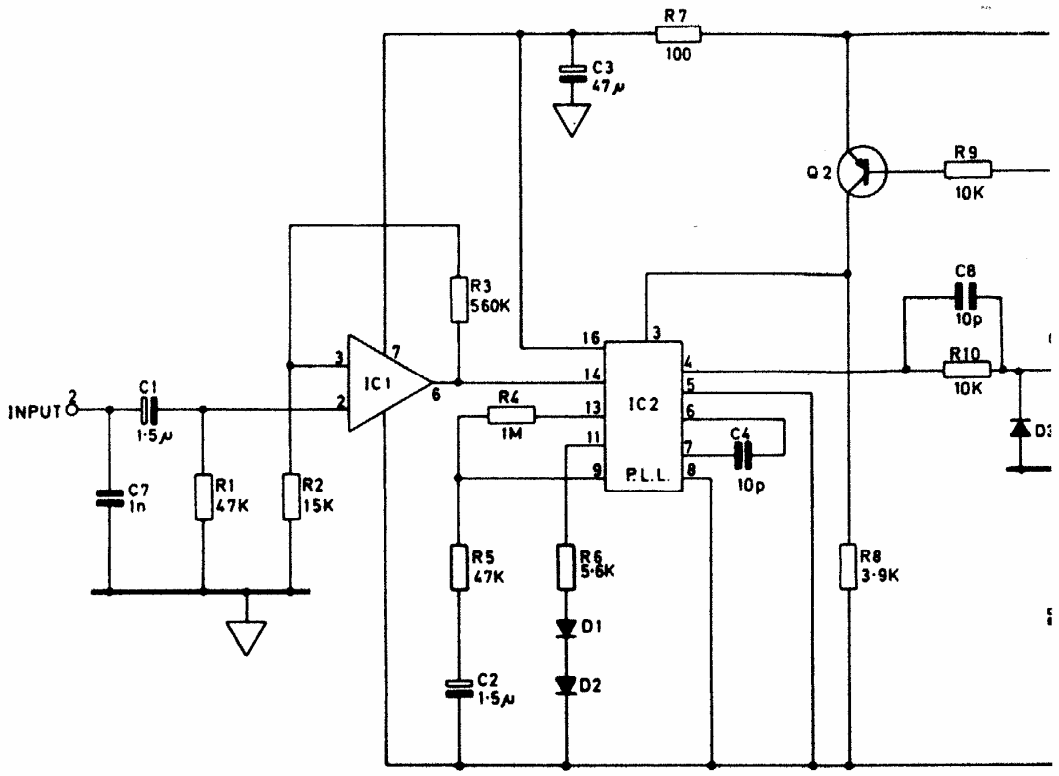
IC REF	+5V PIN	0V PIN
IC 3,14,15,16, 23,21,27,28 30	14	7
IC 7,8,9	16	8
IC 37	-	1, 16

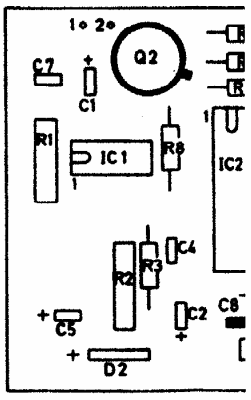
Overall Circuit : 9917
(Part 1) **Fig. 4**


PART OF MAIN PC B ASSY.
19-0808
+5v
C46 100n
C47 10n
C48 47µ
C49 47µ
SPARE
MULTIPLIER SELECT
CHANNEL 'B' BURST
DATA SELECT
L.E.D CHECK
TIE UP
MAIN GATE
CHANNEL A/B
CHANNEL 'A' BURST
CARRY
CLEAR
1. WHEN LF MULTIPLIER SELECTED
(TINUED ROM IG. 4
UP DATE
1PPS
DATA
A
B
C
D
CHANNEL A +'1'
CHANNEL B +0
CHANNEL SELECTED
EXT. STD. INPUT
C57 1n
MAIN GATE
A CHANNEL INPUT
LATCH/UNLATCH
HOLD RESET
EXT. STANDARD INPUT
+2v
V REF
COI CHIP
IC13
GATE CONTROL
10 KHz
HOLD RESET
OVER
MAIN
DATA OUTPUT
EXT. HOLD
EXT. RESET
OPTION
044-9442
043-9421
TO PIN 11
TO PIN 10
19-0834
5 MHz OSCILLATOR ASSY
(Fig. 2
MODE SWITCH S52
BURST
NORM
CHECK SELECT TO R133 (FIG. 4)
CHECK/OPERATE/RESET SWITCH S50
RESET
OPERATE
CHECK
S1R
S1F
GATE TIME SWITCH S1
0·01s
0·1s
1s
10s



Overall Circuit : 9917 (Part 2) Fig.





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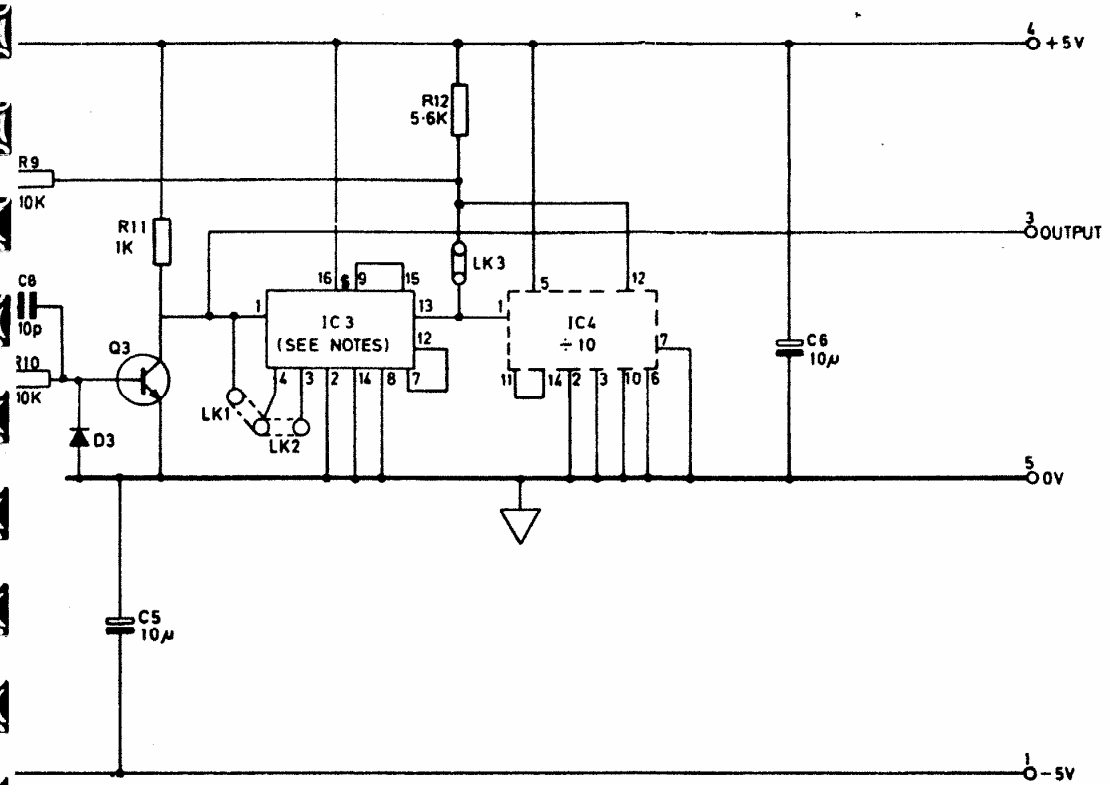

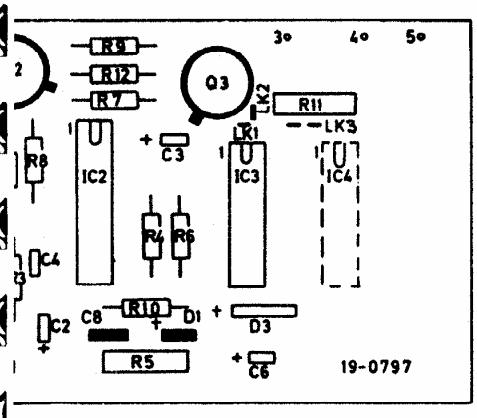

NOTES : 1. LK1 FITTED ON 9911, 9912, 9919 (IC3 ÷ 5)

2. LK2 FITTED ON 9913, 9914, 9915, 9916, 9917, 9917A, 9918, 9921. } IC3 ÷ 10

3 LK3 FITTED ON ALL ABOVE MODELS.

4 IC4 NOT NORMALLY FITTED.

5 THIS VERSION OF 19-0791 IS FITTED IN LATER MODELS. FOR EARLIER MODELS REFER TO ISSUE 1

Circuit and Layout : LF Multiplier Assembly Fig. 6